Appendix I Revision History

Date	Revision	change
2021-01-18	0.0.1	Initial release.

1 GPIO Management

1.1 GPIO general control register

Register 1- 1 GPIOA: Port A data Register

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused
7:0	GPIOA	WR	0x00	PAx data. Valid when PAx is used as GPIO 0: PAx is input low state when read and output low at PAx when write; 1:PAx is input high state when read and output high at PAx when write

Register 1- 2 GPIOASET: Port A Set output data Register

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused
7:0	GPIOASET	WO	X	Set PAx output data. Write 1 set output data. Write 0 affect nothing.

Register 1- 3 GPIOACLR: Port A clear output data Register

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused
7:0	GPIOACLR	WO	X	Clear PAx output data. Write 1 clear output data. Write 0 affect nothing.

Register 1- 4 GPIOADIR: Port A direction Register

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused
7:0	GPIOADIR	WR	0xFF	PAx direction control 0: Output 1: Input

Register 1- 5 GPIOAPU: Port A pull-up register Register

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused
7:0	GPIOAPU	WR	0x0	PAx 10KΩ pull-up resister control. Valid when PAx is used as input 0: disable 1: enable

Register 1- 6 GPIOAPD: Port A pull-down resister Register

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused
7:0	GPIOAPD	WR	0x0	PAx 10KΩ pull-down resister control. Valid when PAx is used as input 0: disable 1: enable

Register 1- 7 GPIOAPU200K: Port A pull-up resister Register

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused
7:0	GPIOAPU	WR	0x0	PAx 200KΩ pull-up resister control. Valid when PAx is used as

Bit	Name	Mode	Default	Description
				input 0: disable 1: enable

Register 1- 8 GPIOAPD200K: Port A pull-down resister Register

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused
7:0	GPIOAPD	WR	0x0	PAx 200KΩ pull-down resister control. Valid when PAx is used as input 0: disable 1: enable

Register 1- 9 GPIOAPU300: Port A pull-up resister Register

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused
7:0	GPIOAPU	WR	0x0	PAx 300Ω pull-up resister control. Valid when PAx is used as input 0: disable 1: enable

Register 1- 10 GPIOAPD300: Port A pull-down resister Register

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused
7:0	GPIOAPD	WR	0x0	PAx 300Ω pull-down resister control. Valid when PAx is used as input 0: disable 1: enable

Register 1- 11 GPIOADE: Port A digital function enable register

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused
7:0	GPIOADE	WR	0xFF	PAx digital function enable 0: Port used as analog IO 1: Port used as digital IO

Register 1- 12 GPIOAFEN: Port A function mapping enable register

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused
7:0	GPIOAFEN	WR	0xFF	PAx function mapping enable 0: Port used as GPIO 1: Port used as function IO

Register 1- 13 GPIOADRV: Port A output driving select Register

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused
7:0	GPIOADRV	WR	0x0	PAx output driving select 0: 8mA 1: 32mA

1.2 GPIO function mapping

Register 1- 14 FUNCMCON0: Port function mapping control Register 0

Bit	Name	Mode	Default	Description
31:28	UT1RXMAP	WR	0x0	UART1 RX mapping 0000: no affect 0001: map to G1

Bit	Name	Mode	Default	Description
				0010: map to G2 0011: map to TX pin by UT1TXMAP select 1111: Clear these bits Others is reserved
27:24	UT1TXMAP	WR	0x0	UART1 TX mapping 0000: no affect 0001: map to G1 0010: map to G2 1111: Clear these bits Others is reserved
23:20				
19:16				
15:12	UT0RXMAP	WR	0x0	UART0 RX mapping 0000: no affect 0001: map to G1 0010: map to G2 0011: map to G3 0100: map to G4 0101: map to G5 0110: map to G6 0111: map to TX pin by UT0TXMAP select 1111: Clear these bits Others is reserved
11:8	UT0TXMAP	WR	0x0	UART0 TX mapping 0000: no affect 0001: map to G1 0010: map to G2 0011: map to G3 0100: map to G4 0101: map to G5 0110: map to G6 0111: map to G7 1111: Clear these bits Others is reserved
7:4	SPI0MAP	WR	0x0	SPI0 mapping 0000: no affect 0001: map to G1 0010: map to G2 0011: map to G3 1111: Clear these bits Others is reserved
3:0	SD0MAP	WR	0x0	SD0 mapping 0000: no affect 0001: map to G1 0010: map to G2 0011: map to G3 0100: map to G4 0101: map to G5 0110: map to G6 1111: Clear these bits Others is reserved

Register 1- 15 FUNCMCON1: Port function mapping control Register 1

Bit	Name	Mode	Default	Description
31:28				
27:24				
23:20				
19:16				
15:12				
11:8	UT2RXMAP	WR	0x0	UART2 RX mapping

Bit	Name	Mode	Default	Description
				0000: no affect 0001: map to G1 0010: map to G2 0011: map to TX pin by UT2TXMAP select 1111: Clear these bits Others is reserved
7:4	UT2TXMAP	WR	0x0	UART2 TX mapping 0000: no affect 0001: map to G1 0010: map to G2 1111: Clear these bits Others is reserved
3:0				

Register 1- 16 FUNCMCON2: Port function mapping control Register 2

Bit	Name	Mode	Default	Description
31:24	-	-	-	Unused
23:20				
19:16	TMR5MAP	WR	0x0	Timer5 PWM mapping 0000: no affect 0001: map to G1 1111: Clear these bits Others is reserved
15:12	TMR4MAP	WR	0x0	Timer4 PWM mapping 0000: no affect 0001: map to G1 1111: Clear these bits Others is reserved
11:8	TMR3MAP	WR	0x0	Timer3 PWM mapping 0000: no affect 0001: map to G1 1111: Clear these bits Others is reserved
7:4	TMR3CPTMAP	WR	0x0	Timer3 capture Pin mapping 0000: no affect 0001: map to G1 0010: map to G2 0011: map to G3 0100: map to G4 0101: map to G5 0110: map to G6 0111: map to G7 1111: Clear these bits Others is reserved
3:0				

1.3 External Port interrupt wake up

Support eight wakeup source input, as the following table. Wakeup circuit 6 and wakeup circuit 7 is special for 32 port interrupts wake up.

Port interrupt source is:

Port_intsrc = {PG[4:0], PF[5:0], PE[7:0], PB[4:0], PA[7:0]};

Wakeup source	Wakeup circuit
PA7	Wakeup circuit 0
PB1	Wakeup circuit 1

PB2	Wakeup circuit 2
PB3	Wakeup circuit 3
PB4	Wakeup circuit 4
WKO	Wakeup circuit 5
PORT_INT_FALL	Wakeup circuit 6
PORT_INT_RISE	Wakeup circuit 7

Register 1- 17 WKUPCON: Wake up control Register

Bit	Name	Mode	Default	Description
31:17	-	-	-	Unused
16	WKIE	WR	0	Wake up interrupt enable 0: disable 1: enable
15:8	-	-	-	Unused
7:0	WKEN	WR	0x0	Wake up input 7~0 enable 0: disable 1: enable

Register 1- 18 WKUPEDG: Wake up edge select Register

Bit	Name	Mode	Default	Description
31:24	-	-	-	Unused
23:16	WKPND	R	0x0	Wake up input 7~0 pending 0: no pending 1: wake up pending
15:8	-	-	-	Unused
7:0	WKEDG	WR	0x0	Wake up input 7~0 wakeup edge select 0: rising edge 1: falling edge

Register 1- 19 WKUPCPND: Wake up clear pending Register

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused
23:16	WKCPND	W	0x0	Wake up input 7~0 clear pending 0: no affect 1: clear wake up pending
15:0	-	-	-	Unused

Register 1- 20 PORTINTEN: Port interrupt enable Register

Bit	Name	Mode	Default	Description
31:0	PORTINTEN	WR	0x0	Port interrupt 0~31 enable bit 0: disable 1: enable

Register 1- 21 PORTINTEDG: Port interrupt edge select Register

Bit	Name	Mode	Default	Description
31:0	PORTINTEDG	WR	0x0	Port interrupt 0~31 edge select bit 0: rise edge 1: fall edge

2 Timer

2.1 Features

1. Timer0/1/2, only support 32bit timer function
2. Timer3/4/5, can be configured to Timer-mode, Counter-mode, Capture-mode and PWM-mode

2.2 Timer0/1/2 Special Function Registers

Register 2- 1 TMR0CON/TMR1CON/TMR2CON: Timer0/1/2 ControlRegister

Bit	Name	Mode	Default	Description
31:10	-	-	-	Unused
9	TPND	WR	0	Timer overflow pending 0: not overflow 1: overflow
8	-	-	-	Unused
7	TIE	WR	0	Timer overflow interrupt enable 0: disable 1: enable
6	INCSRC	WR	0	Increase source select 0: select TMR_INC 1: select external PIN
5:4	-	-	-	Unused
3:2	INCSEL	WR	0x0	Increase clock selection 00: System Clock 01: Counter input rising 10: Counter input falling 11: Counter input edge
1	-	-	-	Unused
0	TMREN	WR	0	Timer Enable Bit 0: Disable 1: Enable

Register 2- 2 TMR0CPND/TMR1CPND/TMR2CPND: Timer0/1/2 clear pending Register

Bit	Name	Mode	Default	Description
31:16	-	-	-	Unused
9	TPCLR	W	0	Timer overflow pending clear bit 0: inactive 1: clear pending
8:0	-	-	-	Unused

Register 2- 3 TMR0CNT/TMR1CNT/TMR2CNT: Timer0/1/2 counter Register

Bit	Name	Mode	Default	Description
31:0	TMRCNT	WR	0x0	Timer counter. TMRCNT will increase when timer is enabled. It overflows when TMRCNT = TMRPR, TMRCNT will be clear to 0x0000 when overflow, and the interrupt flag will be set '1'.

Register 2- 4 TMR0PR/TMR1PR/TMR2PR: Timer0/1/2 period Register

Bit	Name	Mode	Default	Description

Bit	Name	Mode	Default	Description
31:0	TMRPR	WR	0xffffffff	Timer period = TMRPR + 1

2.3 Timer3/4/5 Special Function Registers

Register 2- 5TMR3CON/TMR4CON/TMR5CON: Timer3/4/5 Control Register

Bit	Name	Mode	Default	Description
31:18	-	-	-	Unused
17	CPND	WR	0	Timer capture pending 0: not capture 1: capture
16	TPND	WR	0	Timer overflow pending 0: not overflow 1: overflow
15:12	-	-	-	Unused
11	PWM2EN	WR	0	Timer pwm2 enable bit 0: disable 1: enable
10	PWM1EN	WR	0	Timer pwm1 enable bit 0: disable 1: enable
9	PWM0EN	WR	0	Timer pwm0 enable bit 0: disable 1: enable
8	CIE	WR	0	Timer capture interrupt enable 0: disable 1: enable
7	TIE	WR	0	Timer overflow interrupt enable 0: disable 1: enable
6	INCSRC	WR	0	Increase source select 0: select TMR_INC 1: select external PIN
5:4	CPTEDSEL	WR	0x0	Timer Capture edge select 00: No Capture 01:Capture PIN rising edge 10: Capture PIN falling edge 11: Capture PIN edge
3:2	INCSEL	WR	0x0	Increase clock selection 00: System Clock 01: Counter input rising 10: Counter input falling 11: Counter input edge
1	CPTEN	WR	0	Timer capture Enable Bit 0: Disable 1: Enable
0	TMREN	WR	0	Timer Enable Bit 0: Disable 1: Enable

Register 2- 6 TMR3CPND/TMR4CPND/TMR5CPND: Timer3/4/5 clear pending Register

Bit	Name	Mode	Default	Description
31:18	-	-	-	Unused
17	CPCLR	W	0	Capture pending clear bit 0: inactive 1: clear pending
16	TPCLR	W	0	Timer overflow pending clear bit 0: inactive

Bit	Name	Mode	Default	Description
				1: clear pending
15:0	-	-	-	Unused

Register 2- 7 TMR3CNT/TMR4CNT/TMR5CNT: Timer3/4/5 counter Register

Bit	Name	Mode	Default	Description
31:0	TMRCNT	WR	0x0	Timer counter. TMRCNT will increase when timer is enabled. It overflows when TMRCNT = TMRPR, TMRCNT will be clear to 0x0000 when overflow, and the interrupt flag will be set '1'.

Register 2- 8 TMR3PR/TMR4PR/TMR5PR: Timer3/4/5 period Register

Bit	Name	Mode	Default	Description
31:0	TMRPR	WR	0xffffffff	Timer period = TMRPR + 1

Register 2- 9 TMR3CPT/TMR4CPT/TMR5CPT: Timer3/4/5 capture value Register

Bit	Name	Mode	Default	Description
31:0	TMRCPT	R	x	Timer capture value

Register 2- 10 TMR3DUTY0/TMR4DUTY0/TMR5DUTY0: Timer3/4/5 pwm0 duty Register

Bit	Name	Mode	Default	Description
31:16	-	-	-	Unused
15:0	TMRDUTY0	W	x	Timer pwm0 duty PWM0 low level length is TMRDUTY0+1 PWM 0 high level length is TMRPR-TMRDUTY0+1

Register 2- 11 TMR3DUTY1/TMR4DUTY1/TMR5DUTY1: Timer3/4/5 pwm1 duty Register

Bit	Name	Mode	Default	Description
31:16	-	-	-	Unused
15:0	TMRDUTY1	W	x	Timer pwm1 duty PWM1 low level length is TMRDUTY1+1 PWM1 high level length is TMRPR-TMRDUTY1+1

Register 2- 12 TMR3DUTY2/TMR4DUTY2/TMR5DUTY2: Timer3/4/5 pwm2 duty Register

Bit	Name	Mode	Default	Description
31:16	-	-	-	Unused
15:0	TMRDUTY2	W	x	Timer pwm2 duty PWM2 low level length is TMRDUTY2+1 PWM2 high level length is TMRPR-TMRDUTY2+1

3 IR receiver

3.1 IR RX Special Function Registers

Register 3- 1 IRRXCON: IR RX Control Register

Bit	Name	Mode	Default	Description
31:18	-	-	-	Unused
17	KEYRELS	R	0	IR key release pending 0: not release 1: key release pending
16	RXPND	R	0	IR RX data finish pending 0: not finish 1: finish
15:4	-	-	-	Unused
3	IR32KSEL	WR	0	IR RX 32K configure select 0: 1M clock select 1: 32K clock select
2	IRRXSEL	WR	0	IR RX data select 0: 32bit data 1: 16bit data
1	IRIE	WR	0	IR RX interrupt enable 0: disable 1: enable
0	IREN	WR	0	IR RX enable 0: disable 1: enable

Register 3- 2 IRRXCPND: IRRX clear pending Register

Bit	Name	Mode	Default	Description
31:18	-	-	-	Unused
17	CRELSPND	W	0	Clear key release pending 0: no affect 1: clear pending
16	CRXPND	W	0	Clear RX finish pending 0: no affect 1: clear pending
15:0	-	-	-	Unused

Register 3- 3 IRRXDAT: IRRX data Register

Bit	Name	Mode	Default	Description
31:0	RXDAT	R	0	IR RX data

Register 3- 4 IRRXERR0: IR RX error configure Register0

Bit	Name	Mode	Default	Description
31:28	-	-	-	Unused
27:16	RPTERR	W	0x0	IR repeat time error = (RPTERR + 1) * (1M or 32K)
15:12	-	-	-	Unused
11:0	DATERR	W	0x0	IR data time error = (DATERR + 1) * (1M or 32K)

Register 3- 5 IRRXERR1: IR RX error configure Register1

Bit	Name	Mode	Default	Description
31:20	TOPR	W	0x0	IR time out length = (TOPR + 1) * 64 * (1M or 32K)

Bit	Name	Mode	Default	Description
19:10	ONEERR	W	0x0	IR data 1 time error = (ONEERR + 1) * (1M or 32K)
9:0	ZEROERR	W	0x0	IR data 0 time error = (ZEROERR + 1) * (1M or 32K)

3.2 User Guide

1. Set IR RX bit select
2. Enable IR RX
3. Wait for pending or interrupt
4. Read IRRXDAT or detect RPTPND

4 PWM

4.1 Special Function Registers

Register 4- 1 PWMCON: PMW Configure Register

Bit	Name	Mode	Default	Description
31:5				
5	PWMIVN	WR	0	PWM invert enable 0: duty is high level 1: duty is low level
4	AUTOADJUST	WR	0	PWM Auto Adjust enable 0: disable 1: enable
3	PWM3EN	WR	0	PWM3 enable 0: disable 1: enable
2	PWM2EN	WR	0	PWM2 enable 0: disable 1: enable
1	PWM1EN	WR	0	PWM1 enable 0: disable 1: enable
0	PWM0EN	WR	0	PWM0 enable 0: disable 1: enable

Register 4- 2 PWMPR: PMW period Register

Bit	Name	Mode	Default	Description
31:16				
15:0	PWMPR	WR	0xffff	PWM period = (PWMPR+1) * Tpwmclk

Register 4- 3 PWM01DUT: PWM0/1 duty registers

Bit	Name	Mode	Default	Description
31:16	PWM1DUT	WR	0x0	PWM1 duty register ; Duty = PWM1DUT/ PWMPR
15:0	PWM0DUT	WR	0x0	PWM0 duty register ; Duty = PWM0DUT/ PWMPR

Register 4- 4 PWM23DUT: PWM2/3 duty registers

Bit	Name	Mode	Default	Description
31:16	PWM3DUT	WR	0x0	PWM3 duty register ; Duty = PWM3DUT/ PWMPR
15:0	PWM2DUT	WR	0x0	PWM2 duty register ; Duty = PWM2DUT/ PWMPR

Register 4- 5 PWMCYCNUM: PWM adjust cycle number register

Bit	Name	Mode	Default	Description
31:24	PWM3CYCNUM	WR	0x0	PWM3 Duty adjust cycle num When AUTOADJUST = 1, each PWM3CYCNUM Duty add (PWM3STEP/ PWMPR)
23:16	PWM2CYCNUM	WR	0x0	PWM2 Duty adjust cycle num When AUTOADJUST = 1, each PWM2CYCNUM Duty add (PWM2STEP/ PWMPR)
15:8	PWM1CYCNUM	WR	0x0	PWM1 Duty adjust cycle num When AUTOADJUST = 1, each PWM1CYCNUM Duty add (PWM1STEP/ PWMPR)
7:0	PWM0CYCNUM	WR	0x0	PWM0 Duty adjust cycle num When AUTOADJUST = 1, each PWM0CYCNUM Duty add (PWM0STEP/ PWMPR)

Register 4- 6 PWMSTEP: PWM Step register

Bit	Name	Mode	Default	Description
31:24	PWM3STEP	WR	0x0	PWM3 Duty adjust step
23:16	PWM2STEP	WR	0x0	PWM2 Duty adjust step
15:8	PWM1STEP	WR	0x0	PWM1 Duty adjust step

Bit	Name	Mode	Default	Description
7:0	PWM0STEP	WR	0x0	PWM0 Duty adjust step

5 RTC

5.1 Features

1. Support 32bit Independent power supply real time counter

2. Support alarm interrupt and second interrupt

5.2 Special Function Registers

Register 5- 1RTCCON: RTC Control Register

Bit	Name	Mode	Default	Description
31:13	-	-	-	Unused
20	VUSBONLINE	R	0	VUSB online state 0: not online 1: online
19	RTCWKP	R	0	RTC WK pin state 0: WK pin state is 0 1: WK pin state is 1
18	RTC1SPND	R	0	RTC 1s pending 0: no pending 1: 1s pending
17	ALMPND	R	0	RTC alarm pending 0: no pending 1: alarm pending
16	RTCPND	R	0	RTC trans done 0: done 1:not done
15:9	-	-	-	Unused
8	ALM_WKEN	WR	0	RTC alarm wakeup enable 0: disable 1: enable
7	RTC1S_WKEN	WR	0	RTC 1S wakeup enable 0: disable 1: enable
6	VUSBRSTEN	WR	0	VUSB insert reset system enable 0: disable 1: enable
5	WKUPRSTEN	WR	0	RTC wake up power down mode reset system enable 0: disable 1: enable
4	ALMIE	WR	0	RTC alarm interrupt enable 0: disable 1: enable
3	RTC1SIE	WR	0	RTC 1S interrupt enable 0: disable 1: enable
2:1	BAUDSEL	WR	0x0	Increase clock selection 00: System Clock divide 4 01: System Clock divide 8 10: System Clock divide 16 11: System Clock divide 32
0	RTCCS	WR	0	RTC cs 0:disabled

Bit	Name	Mode	Default	Description
				1:enable

Register 5- 2RTCDAT: RTC data Register

Bit	Name	Mode	Default	Description
31:10	-	-	-	Unused
9:8	RTCMD	W	0x0	RTC cmd 00: data 01: read command 10: write command 11: reserve
7:0	RTCDAT	WR	x	RTC data

Register 5- 3RTCCPND: RTC clear pending Register

Bit	Name	Mode	Default	Description
31:13	-	-	-	Unused
18	C1SPND	R	0	Write 1 will clear RTC 1S pending
17	CALMPND	R	0	Write 1 will clear RTC alarm pending
16:0	-	-	-	Unused

5.3 Independent Power RTC Registers

Register 5- 4 RTCCNT: RTC counter Register

Bit	Name	Mode	Default	Description
31:0	RTCCNT	WR	0x0	32bit RTC counter

Register 5- 5 RTCALM: RTC alarm Register

Bit	Name	Mode	Default	Description
31:0	RTCALM	WR	0xffffffff	32bit RTC alarm

Register 5- 6 RTCRAM: RTC ram Register

Bit	Name	Mode	Default	Description
31:0	RTCRAM	WR	x	64Byte RTCRAM

Register 5- 7 RTCCON0: RTC control Register 0

Bit	Name	Mode	Default	Description
7	PWRUP1ST	WR	1	RTC first power up flag 0: not first power up 1: first power up
6	EXT32KS	WR	0	External 32K select 0: use RTC internal 32K osc 1: use external 32K osc
5	RTCVDDEN	WR	1	RTC VDD12 enable bit 0: disable 1: enable
4	BGEN	WR	0	BG enable bit 0: disable 1: enable
3	LVDOE	WR	0	LVD output enable bit 0: disable 1: enable
2	LVDEN	WR	0	LVD enable bit 0: disable 1: enable
1	X32KEN	WR	0	XOSC32K enable bit 0: disable

Bit	Name	Mode	Default	Description
				1: enable
0	RCEN	WR	0	RCOSC enable bit 0: disable 1: enable

Register 5- 8 RTCCON1: RTC control Register 1

Bit	Name	Mode	Default	Description
7	LVDOUT	R	0	LVD output state 0: LVD state is 0 1: LVD state is 1
6	VRTCEN	WR	0	VRTC enable bit, VRTC voltage for ADC 0: disable 1: enable
5	WKPAEN	WR	0	WK pin analog enable bit, output WKO voltage for ADC 0: disable 1: enable
4	WKPPUEN	WR	1	WK pin pull up enable bit 0: disable 1: enable
3:2	WKPPUS	WR	0x1	WK pin pull up select bit 00: 80K 01: 90K 10: 100K 11: 400K
1	WKPPD	WR	0	WK pin pull down 10K enable bit 0: disable 1: enable
0	WKPIE	WR	1	WK pin input enable bit 0: disable 1: enable

Register 5- 9 RTCCON2: RTC control Register 2

Bit	Name	Mode	Default	Description
7	32KSEL	WR	0	32K osc select bit 0: 32.768K 1: 32K
6	SELVDDPU	WR	1	SEL VDD pullup enable 0: disable 1: enable
5:4	RSV	WR	0x0	Reserve,can't be changed default value
3:2	RSV	WR	0x2	Reserve,can't be changed default value
1:0	RSV	WR	0x2	Reserve,can't be changed default value

Register 5- 10 RTCCON3: RTC control Register 3

Bit	Name	Mode	Default	Description
7	RTC1S_WKEN	WR	0	RTC one second wakeup enable bit 0: disable 1: enable
6	ALM_WKEN	WR	0	RTC alarm wakeup enable bit 0: disable 1: enable
5	VSUB_WKEN	WR	0	VUSB wake up enable bit 0: disable 1: enable
4	WKP_WKEN	WR	0	WK pin wake up enable bit 0: disable 1: enable
3	-	-	-	Unused
2	VCOREEN	WR	1	VDDCORE enable bit

Bit	Name	Mode	Default	Description
				0: disable 1: enable
1	VIOEN	WR	1	VDDIO enable bit 0: disable 1: enable
0	BUCKEN	WR	1	BUCK enable bit 0: disable 1: enable

Register 5- 11 RTCCON5: RTC control Register 5

Bit	Name	Mode	Default	Description
7	-	-	-	Unused
6	RSV	WR	0	Reserve,can't be changed default value
5:4	RSV	WR	0x0	Reserve,can't be changed default value
3:2	RSV	WR	0x0	Reserve,can't be changed default value
1	BUCKLPM	WR	0	BUCK low power mode enable 0: disable 1: enable
0	LDOM	WR	1	BUCK LDO mode select bit 0: buck mode 1: LDO mode

Register 5- 12 RTCCON7: RTC control Register 7

Bit	Name	Mode	Default	Description
7:5	-	-	-	Unused
4	WKOPRT	WR	0	WKO protect bit
3	LVDDETEN	WR	0	LVD detect enable after power up by wake up 0: disable 1:enable
2	WKPFEN	WR	0	WK pin filter enable bit 0: disable 1:enable
1:0	WKPFSEL	WR	0x0	WK pin filter select bit 00:8ms 01:32ms 10:128ms 11:512ms

Register 5- 13 RTCCON8: RTC control Register 8

Bit	Name	Mode	Default	Description
7:5	-	-	-	Unused
4	VSUBP	R	0	VUSB wake up pending 0: no pending 1: pending
3	WKP	R	0	WK pin wake up pending 0: no pending 1: pending
2	RTC1SPC	WR	0	When write: RTC 1 second pending clear 0: no affect 1: clear 1s pending When read: RTC 1 second pending 0: no second pending 1: second pending
1	ALMPC	WR	0	When write: RTC alarm pending clear 0: no affect 1: clear alarm pending

Bit	Name	Mode	Default	Description
				When read: Alarm pending 0: no alarm pending 1: alarm pending
0	WKP10SC	WR	0	When write WK pin 10s pending clear 0: no affect 1: clear 10s pending When read: WK pin 10s pending 0: no 10s pending 1: 10s pending

Register 5- 14 RTCCON9: RTC control Register 9

Bit	Name	Mode	Default	Description
7:4	-	-	-	Unused
3:0	WKP10SEN	W	0xa	WK pin 10s reset enable 0xa: disable Others: enable After enable, can't disable.

6 WDT

6.1 WDT Special Function Registers

Register 6- 1 WDTCON: WDT Control Register

Bit	Name	Mode	Default	Description
31	WDTPND	R	0	WDT time out pending 0: no pending 1: pending
30:28	-	-	-	Unused
27:24	TMRSEL_WR	W	0	WDT time select bit write enable When write 0xa, bit20~bit22 can be write to TMRSEL, other value will no affect
23	-	-	-	Unused
22:20	TMRSEL	R	0x4	WDT time select bit 000: 1ms 001: 256ms 010: 512ms 011: 1024ms 100: 2048ms 101: 4096ms 110: 8192ms 111: 16384ms
19:16	WDTCSEL_WR	W	0	WDT clock select When write 0xa, WDTCSEL =0, when write 0x5, WDTCSEL =1. other value will no affect
16	WDTCSEL	R	0	WDT clock select bit 0:RC32K 1:X32K from 26M divider
15:12	WDTIE_WR	W	0	WDT interrupt disable When write 0xa, WDTIE will disable, when write 0x5, WDTIE will enable. other value will no affect
12	WDTIE	R	0	WDT interrupt enable bit 0: Disable 1: Enable
11:8	WDTRSTEN_WR	W	0	WDT reset disable When write 0xa, WDTRSTEN will disable, other value will no affect
8	WDTRSTEN	WR	1	WDT reset enable bit 0: Disable 1: Enable
7:4	WDTEN_WR	W	0	WDT disable When write 0xa, WDTEN will disable, other value will no affect
4	WDTEN	WR	1	WDT enable bit 0: Disable 1: Enable
3:0	WDTCLR	W	0	WDT clear bit When write 0xa, WDT counter and WDTPND will be clear

6.2 User Guide

1. configure WDT reset or interrupt

2. Select WDT time out

3. Clear WDT

7 SARADC_CTL

7.1 Features

1. Support 16 channel;
2. The maximum sample rate is 78k/s; SARADC bit clock maximum is 1MHz;
3. ADC has internal 100K pull up resister.

7.2 SARADC_CTL Special Function Registers

Register 7- 1 SADCCON: SARADC Control Register

Bit	Name	Mode	Default	Description
31:19	-	-	-	Unused
18	ADCANGIO	WR	0	Saradc auto enable analog IO enable bit 0: Disable 1: Enable
17	ADCIE	WR	0	Saradc interrupt enable bit 0: Disable 1: Enable
16	ADCEN	WR	0	Saradc enable bit 0: Disable 1: Enable
15	CH15PUEN	WR	0	Channel 15 internal pullup enable bit 0: Disable 1: Enable
14	CH14PUEN	WR	0	Channel 14 internal pullup enable bit 0: Disable 1: Enable
13	CH13PUEN	WR	0	Channel 13 internal pullup enable bit 0: Disable 1: Enable
12	CH12PUEN	WR	0	Channel 12 internal pullup enable bit 0: Disable 1: Enable
11	CH11PUEN	WR	0	Channel 11 internal pullup enable bit 0: Disable 1: Enable
10	CH10PUEN	WR	0	Channel 10 internal pullup enable bit 0: Disable 1: Enable
9	CH9PUEN	WR	0	Channel 9 internal pullup enable bit 0: Disable 1: Enable
8	CH8PUEN	WR	0	Channel 8 internal pullup enable bit 0: Disable 1: Enable
7	CH7PUEN	WR	0	Channel 7 internal pullup enable bit 0: Disable 1: Enable
6	CH6PUEN	WR	0	Channel 6 internal pullup enable bit 0: Disable 1: Enable

Bit	Name	Mode	Default	Description
5	CH5PUEN	WR	0	Channel 5 internal pullup enable bit 0: Disable 1: Enable
4	CH4PUEN	WR	0	Channel 4 internal pullup enable bit 0: Disable 1: Enable
3	CH3PUEN	WR	0	Channel 3 internal pullup enable bit 0: Disable 1: Enable
2	CH2PUEN	WR	0	Channel 2 internal pullup enable bit 0: Disable 1: Enable
1	CH1PUEN	WR	0	Channel 1 internal pullup enable bit 0: Disable 1: Enable
0	CH0PUEN	WR	0	Channel 0 internal pullup enable bit 0: Disable 1: Enable

Register 7- 2 SADCCH: SARADC channel enable Register

Bit	Name	Mode	Default	Description
31:17	-	-	-	Unused
16	ADCPND	WR	0	Saradc finish pending 0:Not finish 1:Finish Write SARADCH register will clear this bit
15	CH15EN	WR	0	Channel 15 enable bit 0: Disable 1: Enable
14	CH14EN	WR	0	Channel 14 enable bit 0: Disable 1: Enable
13	CH13EN	WR	0	Channel 13 enable bit 0: Disable 1: Enable
12	CH12EN	WR	0	Channel 12 enable bit 0: Disable 1: Enable
11	CH11EN	WR	0	Channel 11 enable bit 0: Disable 1: Enable
10	CH10EN	WR	0	Channel 10 enable bit 0: Disable 1: Enable
9	CH9EN	WR	0	Channel 9 enable bit 0: Disable 1: Enable
8	CH8EN	WR	0	Channel 8 enable bit 0: Disable 1: Enable
7	CH7EN	WR	0	Channel 7 enable bit 0: Disable 1: Enable
6	CH6EN	WR	0	Channel 6 enable bit 0: Disable 1: Enable
5	CH5EN	WR	0	Channel 5 enable bit 0: Disable 1: Enable
4	CH4EN	WR	0	Channel 4 enable bit

Bit	Name	Mode	Default	Description
				0: Disable 1: Enable
3	CH3EN	WR	0	Channel 3 enable bit 0: Disable 1: Enable
2	CH2EN	WR	0	Channel 2 enable bit 0: Disable 1: Enable
1	CH1EN	WR	0	Channel 1 enable bit 0: Disable 1: Enable
0	CH0EN	WR	0	Channel 0 enable bit 0: Disable 1: Enable

Register 7- 3 SADCST: SAR ADC setup timing Register

Bit	Name	Mode	Default	Description
31:30	CH15ST	WO	0x0	Channel 15 setup time 00:0 SARADC_CLK 01:2 SARADC_CLK 10: 4 SARADC_CLK 11: 8 SARADC_CLK
29:28	CH14ST	WO	0x0	Channel 14 setup time 00:0 SARADC_CLK 01:2 SARADC_CLK 10: 4 SARADC_CLK 11: 8 SARADC_CLK
27:26	CH13ST	WO	0x0	Channel 13 setup time 00:0 SARADC_CLK 01:2 SARADC_CLK 10: 4 SARADC_CLK 11: 8 SARADC_CLK
25:24	CH12ST	WO	0x0	Channel 12 setup time 00:0 SARADC_CLK 01:2 SARADC_CLK 10: 4 SARADC_CLK 11: 8 SARADC_CLK
23:22	CH11ST	WO	0x0	Channel 11 setup time 00:0 SARADC_CLK 01:2 SARADC_CLK 10: 4 SARADC_CLK 11: 8 SARADC_CLK
21:20	CH10ST	WO	0x0	Channel 10 setup time 00:0 SARADC_CLK 01:2 SARADC_CLK 10: 4 SARADC_CLK 11: 8 SARADC_CLK
19:18	CH9ST	WO	0x0	Channel 9 setup time 00:0 SARADC_CLK 01:2 SARADC_CLK 10: 4 SARADC_CLK 11: 8 SARADC_CLK
17:16	CH8ST	WO	0x0	Channel 8 setup time 00:0 SARADC_CLK 01:2 SARADC_CLK 10: 4 SARADC_CLK 11: 8 SARADC_CLK
15:14	CH7ST	WO	0x0	Channel 7 setup time 00:0 SARADC_CLK 01:2 SARADC_CLK

Bit	Name	Mode	Default	Description
				10: 4 SARADC_CLK 11: 8 SARADC_CLK
13:12	CH6ST	WO	0x0	Channel 6 setup time 00:0 SARADC_CLK 01:2 SARADC_CLK 10: 4 SARADC_CLK 11: 8 SARADC_CLK
11:10	CH5ST	WO	0x0	Channel 5 setup time 00:0 SARADC_CLK 01:2 SARADC_CLK 10: 4 SARADC_CLK 11: 8 SARADC_CLK
9:8	CH4ST	WO	0x0	Channel 4 setup time 00:0 SARADC_CLK 01:2 SARADC_CLK 10: 4 SARADC_CLK 11: 8 SARADC_CLK
7:6	CH3ST	WO	0x0	Channel 3 setup time 00:0 SARADC_CLK 01:2 SARADC_CLK 10: 4 SARADC_CLK 11: 8 SARADC_CLK
5:4	CH2ST	WO	0x0	Channel 2 setup time 00:0 SARADC_CLK 01:2 SARADC_CLK 10: 4 SARADC_CLK 11: 8 SARADC_CLK
3:2	CH1ST	WO	0x0	Channel 1 setup time 00:0 SARADC_CLK 01:2 SARADC_CLK 10: 4 SARADC_CLK 11: 8 SARADC_CLK
1:0	CH0ST	WO	0x0	Channel 0 setup time 00:0 SARADC_CLK 01:2 SARADC_CLK 10: 4 SARADC_CLK 11: 8 SARADC_CLK

Register 7- 4 SADCBAUD: SARADC Baud Rate Register

Bit	Name	Mode	Default	Description
31:10	-	-	-	Unused
9:0	SADCBAUD	WO	0x0	SARADC Baud Rate Baud Rate =Fadc clock / [2(SADCBAUD+1)].

Register 7- 5 SADCDAT0~15: SARADC channel 0~15 Data Register

Bit	Name	Mode	Default	Description
31:10	-	-	-	Unused
9:0	SADCDAT	R	0x0	SARADC data, channel 0 to channel 15 register

7.3 User Guide

1. Configure SADCBAUD
2. Configure SADCST if need
3. Enable SARADC

4. Write SADCCH to enable channel to convert. Can enable more than one channel. Write SADCCH will kick start ADC convert.

5. Wait for ADC_PND

8 UART0

8.1 Features

1. UART is a serial port capable of asynchronous transmission.

2. The UART can function in full duplex mode.

8.2 UART0 Special Function Registers

Register 8- 1 UART0CON: UART Control Register

Bit	Name	Mode	Default	Description
31:10	-	-	-	Unused
9	RXPND	R	0	RX pending 0: RX one byte not finish 1: RX one byte finish
8	TXPND	R	0	TX pending 0: TX one byte not finish 1: TX one byte finish
7	RXEN	WR	0	RX enable 0: RX disable 1: RX enable
6	ONELINE	WR	0	One-line mode 0: TX/RX separate 1: TX/RX one line
5	CLKSRC	WR	0	Clock source select 0: system clock 1: uart_inc
4	SB2EN	WR	0	Two Stop Bit enable 0: 1-bit Stop Bit 1: 2 bit Stop Bit
3	TXIE	WR	0	Transmit Interrupt Enable 0 = Transmit interrupt disable 1 = Transmit interrupt enable
2	RXIE	WR	0	Receive Interrupt Enable 0: Receiver interrupt disable 1: Receiver interrupt enable
1	BIT9EN	WR	0	BIT9 Enable Bit 0: Eight-bit mode 1: Nine-bit mode
0	UTEN	WR	0	UART Enable Bit 0: Disable UART module 1: Enable UART module

Register 8- 2 UART0CPND: UART0 clear pending Register

Bit	Name	Mode	Default	Description
31:18	-	-	-	Unused
17	CRSTKEYPND	W	0	Reset Key match pending clear 0: N/A 1: Clear Reset key match Pending
16	CKEYPND	W	0	Key match pending clear 0: N/A 1: Clear key match Pending

Bit	Name	Mode	Default	Description
15:10	-	-	-	Unused
9	CRXPND	W	0	RX pending clear 0: N/A 1: Clear RX Pending
8	CTXPND	W	0	TX pending clear 0: N/A 1: Clear TX Pending. Writing data to UTBUF will clear TXPND
7:0	-	-	-	Unused

Register 8- 3 UART0BAUD: UART Baud Rate Register

Bit	Name	Mode	Default	Description
31:16	UART0RXBAUD	W	0	UART RX Baud Rate Baud Rate =Fsys clock / (UART0RXBAUD + 1)
15:0	UART0TXBAUD	W	0	UART TX Baud Rate Baud Rate =Fsys clock / (UART0TXBAUD + 1)

Register 8- 4 UART0DATA: UART Data Register

Bit	Name	Mode	Default	Description
31:9	-	-	-	Unused
8	UART0BIT8	WR	x	UART Data bit 8
7:0	UART0DAT	WR	x	UART Data Write this register will load the data to transmitter buffer. Read this register will read the data from the receiver buffer..

8.3 User Guide

1. Set IO in the correct direction.
2. Configure UART0BAUD to choose sample rate
3. Enable UART0 by setting
4. Set TXIE or RXIE ‘to 1’ if needed
5. write data to UART0DATA
6. Wait for PND to change to ‘1’, or wait for interrupt
7. Read received data from UART0DATA if needed

9 SD_CTL

9.1 Features

The crown system's SD card host controller can support SD/MMC card devices.

1. SD memory Card Spec (Ver2.0) / MMC Spec (Ver4.3) compatible;

2. CRC7 and CRC16 Generator;

3. Support Interrupt and DMA Data transfer mode;

4. Support 1-bit or 4-bit data bus width;

5. Support up to 50MHz in data transfer mode for SD;

6. Support up to 50MHz in data transfer mode for MMC.

9.2 Special Function Registers

Register 9- 1 SD0CON: SD0 Control Register

Bit	Name	Mode	Default	Description
31:21	-	-	-	Unused
20	BUSY	R	0	Busy flag, The logic level of pad DAT0 0: device busy 1: device not busy
19:17	CRCS	R	X	CRC status for sent data packet 101: Error transmission 010: Non-erroneous transmission 111: Flash error
16	DCRCE	R	0	Read Data CRC error flag 0: no error 1: error detected
15	NRPS	R	0	No response received 0: Response received 1: No response received
14	CCRCE	R	0	Command CRC error 0: no error 1: error detected
13	DFLAG	R	0	Data finish flag 0: Send or Receive data not finish 1: Send or Receive data finish
12	CFLAG	R	0	Command finish flag 0: Send command or Receive response not finish 1: Send command or Receive response finish
11:7	-			
6	CLKIDLE	WR	1	SD CLK idle state select 0: SD CLK idle state is 0 1: SD CLK idle state is 1
5	DATIE	WR	0	Data interrupt enable bit 0: disable 1: enable
4	CMDIE	WR	0	Command interrupt enable bit

Bit	Name	Mode	Default	Description
				0: disable 1: enable
3	CKEN	WR	0	SD clock always output enable 0: disable 1: keep clock output
2	OUTEDGE	WR	0	SD host senddataor command edge selection 0: falling edge output 1: rising edge output
1	DWTH	WR	0	Data bus width 0: 1-bit mode 1: 4-bit mode
0	SDEN	WR	0	SD controller enable bit 0: disable 1: enable

Register 9- 2 SD0CPND: SD0 clear pending Register

Bit	Name	Mode	Default	Description
31:14	-	-	-	Unused
13	DFCLR	W	0	Data flag clear bit 0: inactive 1: clear pending
12	CFCLR	W	0	Command flag clear bit 0: inactive 1: clear pending
11:0	-	-	-	Unused

Register 9- 3 SD0CMD: SD0 Command Register

Bit	Name	Mode	Default	Description
31:12	-	-	-	Unused
11	CK8E	W	0	Send eight SD clocks after command enable bit 0: disable 1: enable
10	CCBUSY	W	0	Check command busy enable 0: disable 1: enable
9	LRSP	W	0	17-byte long response enable 0: 6byte response 1: 17byte response
8	RSPEN	W	0	Response enable 0: disable 1: enable
7:0	SDCMD	WR	x	Send command or receive response 8 bit index

Register 9- 4 SD0ARG3: SD0 Argument 3 Register

Bit	Name	Mode	Default	Description
31:0	SDARG3	WR	x	Send command or receive response 32 bit argument

Register 9- 5 SD0ARG2: SD0 Argument 2 Register

Bit	Name	Mode	Default	Description
31:0	SDARG2	R	x	Receive response 32 bit argument

Register 9- 6 SD0ARG1: SD0 Argument 1 Register

Bit	Name	Mode	Default	Description
31:0	SDARG1	R	x	Receive response 32 bit argument

Register 9- 7 SD0ARG0: SD0 Argument 0 Register

Bit	Name	Mode	Default	Description
31:0	SDARG0	R	x	Receive response 32 bit argument

Note: when send command, should write SD0ARG3 as argument; when receive 48bit response, SD0ARG3 is the 32bit argument.

Register 9- 8 SD0BAUD: SD0 Baud Rate Register

Bit	Name	Mode	Default	Description
31:8	-	-	-	Unused
7:0	SDBAUD	W	0	Baud rate control; Can't set zero Baud rate = system clock / (SDBAUD +1)

Register 9- 9 SD0DMAADR: SD0 Data DMA Address Register

Bit	Name	Mode	Default	Description
31:21	-	-	-	Unused
20:0	DADR	W	x	The DMA byte address

Register 9- 10 SD0DMACNT: SD0 Data DMA Counter Register

Bit	Name	Mode	Default	Description
31:19	-	-	-	Unused
18	CK8E	W	0	Send eight SD clocks after data 0: disable 1: enable
17	CDBUSY	W	0	Check data busy when write data to SD card enable 0: disable 1: enable
16	WRD	W	0	Write data to SD card 0: read data from SD card 1: write data to SD card
15:9	-	-	-	Unused
10:0	DCNT	W	0	Write this register to kick start DMA transfer Total number of bytes received / transferred is SDDCNT

9.3 User Guide

Command Operation Flow:

1. Configure SD0ARG3
2. Configure SD0CMD and kick start
3. Wait for CFLAG to become 1 or wait for interrupt. Check CCRCE whether CRC is valid if need
4. Read content of response from SD0CMD and SD0ARG3 if response is 6 bytes. If response is 17 bytes, read from SD0CMD, SD0ARG3, SD0ARG2, SD0ARG1, SD0ARG0

Data Operation:

Sending data Flow:

1. Configure DWTH, OUTEDGE;
2. Prepare sending data and set SD0DMAADR to point to starting address of data.
3. Select data type and Configure SD0DMACNT for the number of sending data.
4. Wait for DFLAG to become 1 or wait for interrupt.
5. Check CRCS to obtain CRC status value from SD device.

6. If CRC status is correct, check BUSY bit until release

Receiving data:

1. Configure DWTH, OUTEDGE

2. Set SD0DMAADR to point to starting address for receiving data

3. Select data type and configure SD0DMACNT for the number of receiving data.

4. Wait for DFLAG to become 1 or wait for interrupt.

5. Check DCRCE to determine whether the data received is right.